Far-End Crosstalk Cancellation in High-Speed Serial Links

R. Harjani (PI), K.-J. Sham, M. R. Ahmadi
Electrical & Computer Engineering, University of Minnesota

- **I/Os are the performance bottleneck in high-speed electronic systems**
- **Project Goal**
  - To develop techniques for mitigating far-end crosstalk (FEXT), a dominant noise source in high-speed I/Os

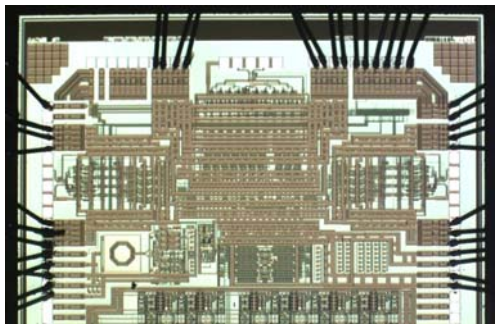

Fig. 1. 10Gbps multi-lane transmitter chip micrograph

- **Results**
  - Successfully implemented FEXT cancellation in a 10Gbps transmitter in 0.18µm CMOS technology
  - Improved timing margin by ~50% and voltage margin by ~15% when reduce spacing by 2X
  - Allow for faster, longer distance, less spacing I/Os

w/o FEXT Cancellation **w/ FEXT Cancellation**

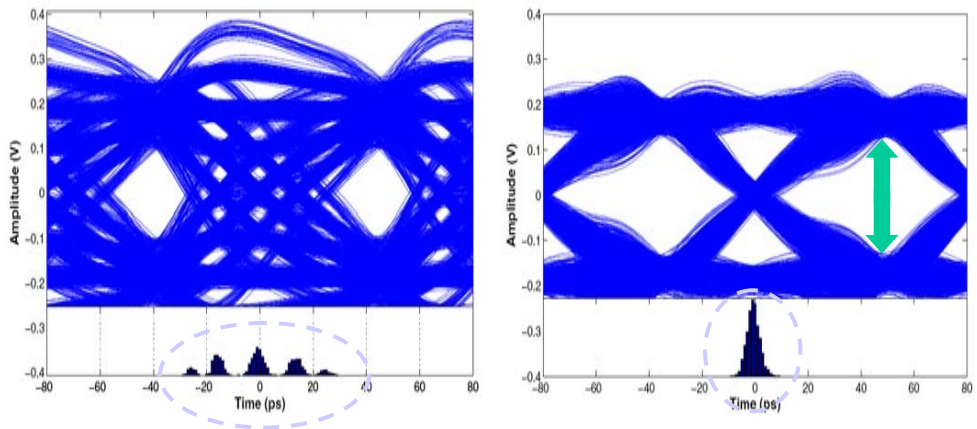

Fig. 2. Eye diagrams & jitter histograms w/ & w/o FEXT cancellation

- **Publications**
  - M. R. Ahmadi, et. al, “A Spur Reduction Technique for Multi-GHz Clock Generators,” (Submitted to 2007 VLSI Symposium).
  - S. Bommalingaiahnapallya, et. al, “A Three-lane Low-power 5Gbps 0.18um CMOS PRBS Generator,” (Submitted to 2007 VLSI Symposium).
  - S. Bommalingaiahnapallya, et. al, “High-Speed Circuits for a Multi-Lane 12Gbps CMOS PRBS Generator,” IEEE ISCAS 2007.
  - K.-J. Sham, et. al, “FEXT Crosstalk Cancellation for High-Speed Serial Link Design,” IEEE CICC 2006.