Novel Integration Technique for Flip-Chip Bonding Circuit in Wafer Scale Packaging

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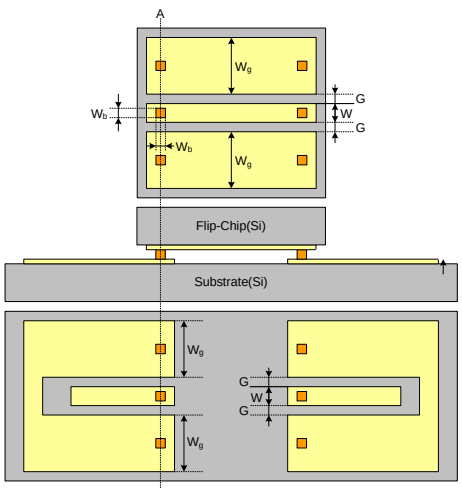
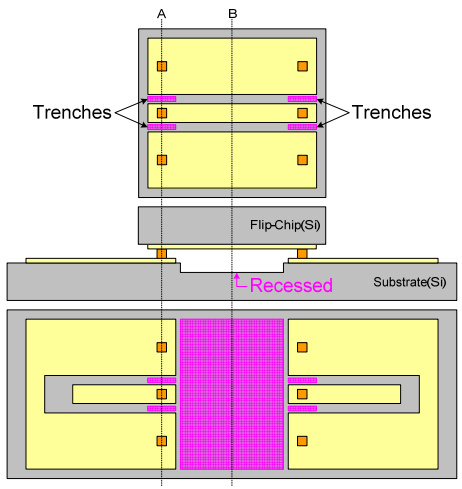
- DESCRIPTION OF WORK
  - Characterization of Au-Sn alloys for flip-chip interconnect
  - Improvement of transmission characteristic of conventional flip-chip interconnect

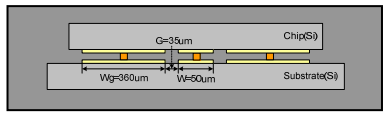


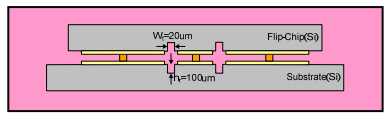
(a) Conventional flip-chip Interconnect

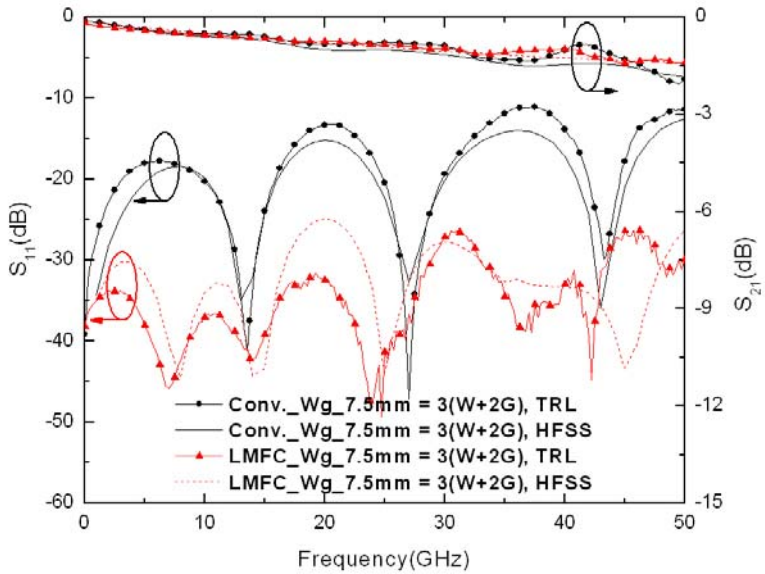


(b) Locally matched flip-chip Interconnect

- MAJOR OBSERVATIONS
  - Return loss is improved by 20dB.
  - Oscillation characteristics in insertion loss are removed in high frequency band.







- Publication
  - Y. S. Cho and R. F. Drayton, “Novel Integration Technique for Flip-Chip Bonding Circuit in Wafer Scale Packaging,” IEEE AP-S International Symposium Digest, vol. 1, pp.57-60, July 2006.