Characterization of Reverse Pulse Plating of Vias for High Frequency Circuits

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- DESCRIPTION OF WORK
  - The goal of this work is to develop a process for via formation using reverse pulse electroplating with copper
  - Vias are etched in silicon, then a thin (.5 um) layer of copper is sputtered on the wafer.
  - Reverse pulse plating is then used to deposit copper on planar surface features and to fill the vias

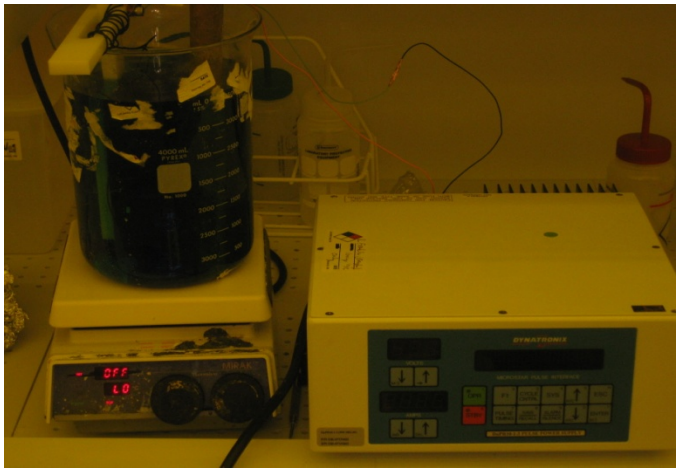

Fig. 1: Plating bath setup showing plating bath and reverse pulse power supply.

Feature	Minimum Thickness (um)	Maximum Thickness (um)	Average Thickness (um)
1	11.6	13.21	12.405
2	12.56	16.6	14.58
3	11.48	13.63	12.555
4	13.29	14.42	13.855
5	11.77	12.77	12.27
6	9.91	12.01	10.96
Average	11.77	13.77	12.77
StD	1.14	1.61	1.17

Fig. 2: Thickness of planar features after 30 minutes of reverse pulse plating.

- MAJOR OBSERVATIONS
  - Reverse pulse plating is slower than standard DC plating, but the features are smoother and more polished
  - Plating rate is about 25 um per hour, will require approximately 8 hours to fill 200 um thick vias